Design of a 256-KBit EEPROM IP for Touch-Screen Controllers

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Abstract—We propose a compact design having low-power and high-speed EEPROM for touch-screen controller ICs. To optimize a small-area EEPROM design, a SSTC (side-wall selective transistor) cell is proposed which involves repeated high-voltage switching circuits inside the EEPROM core circuit. A digital data-bus sensing amplifier circuit is proposed as a low-power technology. For high speed, the distributed data-bus scheme is applied, and the driving voltage for both the EEPROM cell and the high-voltage switching circuits uses VDDP (=3.3V) which is higher than the logic voltage, VDD (=1.8V), using a dual power supply. The layout size of the designed 256-KBit EEPROM IP is 1765.05μm × 691.71μm.

Keywords—EEPROM, Touch-Screen Controller; small-area; low-power; high-speed; asynchronous interface; distributed data bus; digital sensing.

I. INTRODUCTION

Non-volatile memories widely used for touch-screen controllers are OTP (One-time programmable) memories, EEPROMs and flash memories [1][2]. Although OTP memories have been used widely and recently, MTP (Multi-time programmable) memories are more suitable for multiple programming. There are also EEPROMs and flash memories as part of MTP memories. EEPROM memories are more widely used for applications which require a compact size and a memory capacity between 64-KBit to 256-KBit.

Generally, EEPROM IPs for mobile applications require low power and compact area design to reduce market price. In addition, the touch-screen controllers require high speed capabilities of 10MHz. The conventional design technique for low-area EEPROM cell technology involves asynchronous interface method and separated I/O method [3]. Furthermore, Dickson charge pump using Schottky diodes and high-voltage switching circuit have been also proposed as conventional low-power techniques.

In this paper, we propose a compact design having low-power and high-speed 256-KBit EEPROM IP. To optimize a small-area EEPROM design, a SSTC (side-wall selective transistor) cell is proposed which involves repeated high-voltage switching circuits inside the EEPROM core circuit. Low power technique is achieved by having digital data-bus sensing amplifier without a reference voltage generator to be used to reduce its stand-by current. For high speed, the distributed data-bus scheme is applied, and the driving voltage for both the EEPROM cell and the high-voltage switching circuits uses VDDP (=3.3V) which is higher than the logic voltage, VDD (=1.8V), using a dual power supply. The layout size of the designed 256-KBit EEPROM IP is 1765.05μm × 691.71μm.

II. CIRCUIT DESIGN

The design consists of asynchronous 256-KBit EEPROM IP which uses SSTC cells. The Fowler-Nordheim (FN) tunneling method is used to program or erase the EEPROM. The cell size is 1.135μm × 0.88μm (=0.99μm²). The cell array is arranged as 256 rows x 1024 columns. There are two power supplies: VDD (=1.8V) for logic circuits and VDDP (=3.3V) driving EEPROM cells. There are three operation modes: erase, program and read modes. Asynchronous interface and separated I/O are used to reduce the IP size.

As shown in Fig. 1, the 256-KBit EEPROM design consists of an EEPROM cell array of 256 rows × 1024 columns. The word line (WL) driver selects one of 256 WLs by decoding the address bus A[7:0]. The bit line (BL) switch and the write data (WD) switch selects one of 64 word lines (WLs) by decoding the column address bus A[13:8]. Lastly, the WD driver attains the input data and the DB sense amplifier senses and reads out the data from the cells. The DC-DC converter that supplies high voltages to VPP and VPPL permits write functions and the control logic supplies the internal control signals. There are command control signals (including RSTb, RD, ERS and PGM), address bus (A), an input data bus (DIN) and an output data bus (DOUT).

![Figure 1. Block diagram of 256-KBit EEPROM IP.](image-url)
A word of data DIN[15:0] is programmed into the address after the word of selected cells is erased. If ERS is activated to the high state after the address for a word of data is initially applied, the word of data in the selected cells is erased. If PGM is activated to the high state after the address and having the word of data initially applied, the word of data is programmed into the selected cells. If READ mode is activated to the high state after the address for a word of data is applied before, the word of data from the selected cells is outputted on to the DOUT port in tAC (access time). At this stage, ERS and PGM must be kept low and DIN[15:0] is in the don’t-care state.

As shown in Fig. 2, the write data (WD) switch circuit inside the EEPROM core circuit occupies majority of the space. This is due to the HV (High voltage) transistors being integrated into a column pitch of 0.89μm. In this paper, we optimized the size of the HV transistors by using the WD switch circuit to a degree which drives the FN tunneling a maximal current of 10nA. In erase mode, the BLs of the selected word is driven into VPP through WDs and the other BLs of the non-selected word into VPPL. In program mode, the BLs of the selected word is driven to 0V, namely a voltage of WD or VPPL whilst the other BLs of non-selected word is driven to VPPL. The high-VT NMOS transistor connected to BLC_EN preconditions BL to VDD in exiting program mode.

Figure 2. Optimized write data switch circuit.

Fig. 3 shows a proposed read data switch circuit transferring 1024 columns, namely 64 words, of BL data to the data bus lines selected by decoding the address bus A[13:8]. A native transistor which is used in the high voltage range is used to protect from a damage when VPP or VPPL is applied to BL in write mode. A transistor of 5V connected with the native transistor in series is used to reduce an off-leakage current.

Figure 3. Proposed read data switch circuit.

The driving current is increased since the driving voltage for the read data (RD) switch and WL, namely the control gate (CG) of an EEPROM cell, is VDDP in lieu of VDD in a high speed reading mode. As shown in Fig. 4, the distributed data bus (DB) scheme is used to reduce the DB loading capacitance. High speed is obtained by making the junction, the gate-source overlap, and interconnect capacitances by the read data switching transistor of 5V connected to the DB lines about a quarter smaller when compared with the single DB counterpart.

Figure 4. Distributed data bus scheme.

From this, high-speed sensing can be achieved at the digital data bus (DB) sensing circuit [3] and low power is attained by removing the reference voltage generator. Fig. 5 shows the designed DB sensing circuit. It consists of a negative-level sensitive D latch, a low-impedance DB precharging transistor (MP0) and a high-impedance DB load transistor (MP1). Compared with the conventional sensing circuit [4], the digital sensing circuit removes data-fighting events in the D latch. There is an increase in noise margin of the programmed cell since MP1 is always on and coupling noise from the switching of MP1 is removed. A low-power DC-DC converter with Dickson charge pump using Schottky diodes and high-voltage switching circuits is used to recognize low power in write mode.
III. SIMULATION AND EXPERIMENT RESULTS

Based on above, an asynchronous 256-KBit EEPROM IP with MagnaChip's 0.18\(\mu\)m EEPROM process is designed. The switching speed is increased by about 17.3\(\mu\)s since the data bus (DB) load capacitance is almost a quarter smaller when compared to the single DB scheme and the distributed DB counterpart.

Fig. 6 shows the timing diagram for the control signal RD from the EEPROM IP in read mode and the signals PRECHARGE and SAENb from the control logic in Fig. 1. DB precharges to VDD and when a read command enters, BL affects the VDD-VTN by the PRECHARGE signal. If WL is activated and a cell datum is transferred to BL through the BL switch. After BL is precharged, the digital datum of BL is sensed by the DB S/A and outputted to the node DOUT by the signal SAENb. Fig. 6(a) shows a simulation result for a ‘0’-programmed cell and Fig. 6(b) refers to the results from a ‘1’-programmed cell. The access time, \(t_{AC}\), is 85.7\(\mu\)s and the worst case occurred when reading are taken at a datum of ‘1’.

The operational currents of the designed 256-KBit EEPROM IP in read mode are 306.0\(\mu\)A with the supply voltage of VDD of 1.8V and 0.624 \(\mu\)A with the supply voltage of VDDP of 3.3V under the following conditions: temperature = 25\(^\circ\)C and typical model parameters. Fig. 7 shows the layout image of the designed 256-KBit EEPROM IP with MagnaChip’s 0.18\(\mu\)m EEPROM process. The layout size is 1765.05 \(\mu\)m \(\times\) 691.71 \(\mu\)m.

IV. CONCLUSIONS

EEPROM IPs for mobile applications require low power and compact area design to reduce market price. In addition, the touch-screen controllers require high speed capabilities of 10MHz. Thus, we designed a compact design having low-power and high-speed 256-KBit EEPROM IP for touch-screen controllers.

To optimize a small-area EEPROM design, a SSTC (side-wall selective transistor) cell was used which involves repeated high-voltage switching circuits inside the EEPROM core circuit. The layout size is 1765.05 \(\mu\)m \(\times\) 691.71 \(\mu\)m. Low power technique is achieved by having digital data-bus sensing amplifier without a reference voltage generator to be used to reduce its stand-by current. Also, a high speed of 85.7\(\mu\)s was possible when using the distributed data-bus scheme and the dual supply voltage.

REFERENCES


